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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,934	03/06/2002	Amir Alon	IL920020007US1	7058

7590 10/16/2003

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EXAMINER	
LEVIN, NAUM B	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 10/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,934	ALON ET AL.	
	Examiner	Art Unit	
	Naum B Levin	2825	

-- The MAILING DATE of this communication appears on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-9,11-18 and 22-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-9,11-18 and 22-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This office action is in response to application 10/091,934 and Amendment filed on 08/06/2003. Claims 2-9, 11-18, 22-35 remain pending in the application.

Examiner appreciates the detailed remarks offered by Applicant. Based on the remarks and Amendment Examiner has performed additional search, and found a new references.

Claim Objections

2. Claim 31 is objected to because of the following informalities:

In claim 31, line 8 after "at least" insert – including--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 6-9 and 11-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al. (Pub. No.: US 2002/0104063).

Chang discloses method and system for extraction of parasitic interconnect impedance including inductance comprising:

(6) A design topology of critical interconnect lines (p.1, [0006]);

(7) The design topology of claim 6 wherein said topology is predefined (p.1, [0006]);

(8) The topology of claim 6 comprising a definite current return path (p.4, [0043] and p.12, Claim2);

(9) The design topology of claim 6 wherein said topology/models comprises a model describing one or more of said following electrical parameters: capacitance, low frequency inductance, high frequency inductance, low frequency series resistance, high frequency series resistance, TEM impedance, and matrix representations of one or more of said parameters (p.2, [0028] and [0029] and p.3, [0032]; p.3-4, [0041]);

(11) The design topology of claim 6 wherein said topology comprises one or more signal wires and one or more shielding wires (p.7, [0080]);

(12) The design topology of claim 11 wherein said one or more shielding wires is one or more side shielding wires located on one or more sides of said signal wires (p.7, [0082]);

(13) The design topology of claim 11 and wherein said one or more shielding wires is a bottom shielding wire (p.7, [0082]);

(14) The design topology of claim 11 and wherein said one or more shielding wires is one or more shielding layers (p.7, [0082]).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 2-7, 15-18, 22-25 and 28-35 are rejected under 35 U.S.C. 102(b) as as being anticipated by Dangelo et al. (US Patent 5,555,201).

Dangelo teaches method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information comprising:

(2) An integrated circuit design kit comprising:

means for generating one or more circuit components topologies (col.1, ll.58-67; col.2, ll.1-16; col. 16, ll.3-6, ll.13-16 and ll.35-47; col. 17, ll.23-37 and ll.63-67; col. 19, ll.65-67; col. 20, ll.1-12, ll.12-25 and ll.26-30; col. 21, ll.53-67; col. 22, ll.1-4; col. 23, ll.24-42, ll.52-61 and ll.66-67; col. 24, ll.1-2and ll.12-16; col.29, ll.30-40; and col. 66, ll.13-28); and

means for generating one or more critical interconnect lines topologies (col. 16, ll.3-6, ll.13-16 and ll.35-47; col. 17, ll.23-37 and ll.63-67; col. 19, ll.65-67; col. 20, ll.1-12, ll.12-25 and ll.26-30; col. 21, ll.53-67; col. 22, ll.1-4; col. 23, ll.24-42, ll.52-61 and ll.66-67; col. 24, ll.1-2and ll.12-16; col.29, ll.30-40; and col. 66, ll.13-28);

(6) A design topology of critical interconnect lines (col. 16, ll.3-6, ll.13-16 and ll.35-47; col. 17, ll.23-37 and ll.63-67; col. 19, ll.65-67; col. 20, ll.1-12, ll.12-25 and ll.26-30; col. 21, ll.53-67; col. 22, ll.1-4; col. 23, ll.24-42; ll.52-61 and ll.66-67; col.24, ll.1-2 and ll.12-16 and col. 66, ll.13-28);

(7) The design topology of claim 6 wherein said topology is predefined (col. 16, ll.3-6, ll.13-16 and ll.35-47; col. 17, ll.23-37 and ll.63-67; col. 19, ll.65-67; col. 20, ll.1-12, ll.12-25 and ll.26-30; col. 21, ll.53-67; col. 22, ll.1-4; col. 23, ll.24-42, ll.52-61 and ll.66-67; col. 24, ll.1-2and ll.12-16; col.29, ll.30-40; and col. 66, ll.13-28);

(15) A computer software product for designing an integrated circuit, said product comprising a computer readable medium in which program instruction are stored, which, when read by a computer, cause said computer to create a design topology of critical interconnect lines (col.9, ll.11-67; col.10, ll.1-45; col.15, ll.25-47; col. 16, ll.3-6, ll.13-16 and ll.35-47; col. 17, ll.23-37 and ll.63-67; col. 19, ll.65-67; col. 20, ll.1-12, ll.12-25 and ll.26-30; col. 21, ll.53-67; col. 22, ll.1-4; col. 23, ll.24-42; ll.52-61 and ll.66-67; col.24, ll.1-2 and ll.12-16 and col. 66, ll.13-28);

(16) The product of claim 15 and further comprising instructions, which, when read by a computer, cause said computer to create a design model of critical interconnect lines (col.9, ll.11-67; col.10, ll.1-45; col.15, ll.25-47; col. 16, ll.3-6, ll.13-16 and ll.35-47; col. 17, ll.23-37 and ll.63-67; col. 19, ll.65-67; col. 20, ll.1-12, ll.12-25 and ll.26-30; col. 21, ll.53-67; col. 22, ll.1-4; col. 23, ll.24-42; ll.52-61 and ll.66-67; col.24, ll.1-2 and ll.12-16 and col. 66, ll.13-28);

(17) A computer software circuit design product for designing an integrated circuit, said product comprising a computer readable medium in which program instruction are stored, which instructions, when read by a computer, cause said computer to deploy said circuit design product, said circuit design product comprising a

means for designing topology of critical interconnect lines (col.9, ll.11-67; col.10, ll.1-45; col.15, ll.25-47; col. 16, ll.3-6, ll.13-16 and ll.35-47; col. 17, ll.23-37 and ll.63-67; col. 19, ll.65-67; col. 20, ll.1-12, ll.12-25 and ll.26-30; col. 21, ll.53-67; col. 22, ll.1-4; col. 23, ll.24-42; ll.52-61 and ll.66-67; col.24, ll.1-2 and ll.12-16 and col. 66, ll.13-28);

(18) The product of claim 17 and further comprising instructions, which, when read by a computer, cause said computer to create a design model of critical interconnect lines (col.9, ll.11-67; col.10, ll.1-45; col.15, ll.25-47; col. 16, ll.3-6, ll.13-16 and ll.35-47; col. 17, ll.23-37 and ll.63-67; col. 19, ll.65-67; col. 20, ll.1-12, ll.12-25 and ll.26-30; col. 21, ll.53-67; col. 22, ll.1-4; col. 23, ll.24-42; ll.52-61 and ll.66-67; col.24, ll.1-2 and ll.12-16 and col. 66, ll.13-28);

(22) The method of claim 32, wherein said integrated circuits are analog and mixed signal (AMS) circuits or application specific integrated circuits (ASIC) (col.17, ll.15-19);

(23), (29), (33) The method of claim 32, wherein in (b), the step of defining comprises choosing from a set of predefined parameterized topologies (col.73, ll.66-67 and col.74, ll.1-17);

(28) The method according to claim 32, wherein step (b) comprises: using one or more of said following to identify said critical interconnect lines: estimated length, metal level assignment, signal integrity, timing requirements and manual user selection (col.20, ll.26-30; col.43, ll.58-67; col.73, ll.66-67 and col.74, ll.1-17);

(31), (3), (4), (5), (7) A system for integrated circuit design comprising:

means/tools for designing a high level design, said high level circuit design including a chip architecture and a floor plan, whereby major design blocks and their locations are defined/mapping and further including one or more critical interconnect wire topologies (col. 16, ll.3-6, ll.13-16 and ll.35-47; col. 17, ll.23-37 and ll.63-67; col. 19, ll.65-67; col. 20, ll.1-12, ll.12-23 and ll.26-30; col. 23, ll.52-61 and ll.66-67; col. 24, ll.1-2 and col. 66, ll.13-28);

means/tools for designing a schematic design at least including one or more circuit components and one or more critical interconnect wire models (col. 20, ll.23-25; col. 21, ll.53-67; col. 22, ll.1-4; col. 23, ll.24-42 and col.24, ll.12-16); and

means/tools for designing a physical layout at least including said one or more circuit components and said one or more critical interconnect wire topologies (col. 24, ll.58-67 and col. 25, ll.24-29);

(32), (24), (25), (30) A method for designing integrated circuits (IC), said method comprising steps of:

a) defining a chip architecture and a floor plan (col. 16, ll.3-6, ll.13-16 and ll.35-47; col. 17, ll.23-37 and ll.63-67; col. 19, ll.65-67; col. 20, ll.1-12; col. 23, ll.66-67; col. 24, ll.1-2);

b) identifying one or more critical interconnect lines/wire delays and defining one or more transmission line topologies/paths for design of said critical interconnect lines (col. 20, ll.12-23 and ll.26-30; col. 23, ll.52-61 and col. 66, ll.13-28);

c) determining a schematic design/gate level of said IC from said chip

architecture, floor plan and said critical interconnect line topologies (col. 20, ll.23-25; col. 21, ll.53-67; col. 22, ll.1-4; col. 23, ll.24-42 and col.24, ll.12-16); and

d) defining a physical layout of said IC at least from said chip architecture, floor plan and said critical interconnect line topologies (col. 24, ll.58-67 and col. 25, ll.24-29);

(34) A system for integrated circuit design comprising:

means/tools for designing a schematic design at least including one or more circuit components and one or more critical interconnect wire models, wherein said one or more critical interconnect wire models are parameterized cells of on or more transmission line topologies (col.1, ll.58-67; col.2, ll.1-16; col. 20, ll.23-25; col. 21, ll.53-67; col. 22, ll.1-4; col. 23, ll.24-42 and col.24, ll.12-16; col.29, ll.30-40; col.73, ll.66-67 and col.74, ll1-17);

(35) A system for integrated circuit design comprising:

means/tools for designing a schematic design (col. 20, ll.23-25; col. 21, ll.53-67; col. 22, ll.1-4; col. 23, ll.24-42 and col.24, ll.12-16); and

means/tools for designing a physical layout at least including said one or more circuit components and said one or more critical interconnect wire topologies, wherein said one or more critical interconnect wire models are parameterized cells of transmission lines (col. 24, ll.58-67; col. 25, ll.24-29; col.73, ll.66-67 and col.74, ll1-17);

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo in view of Chang.

With respect to claims 26 and 27 Dangelo teaches the features above but lacks a method for designing integrated circuits (ICs) further comprising step of calculating at least one of electrical parameters of IC models, and creating matrix representation for at least one of electrical parameters.

Chang discloses method and system for extraction of parasitic interconnect impedance including inductance comprising:

(26) The method according to claim 25, and further comprising the step of calculating one or more electrical parameters of said models (p.1, [0002] and p.2, [0010]);

(27) The method according to claim 26, wherein said one or more electrical parameters includes one or more of the following: capacitance, low frequency inductance, high frequency inductance, low frequency series resistance, high frequency series resistance, TEM impedance, and matrix representations of one or more of said parameters (p.2, [0028] and [0029]; p.3, [0032] and [0041] and p.4, [0042]).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Chang's teaching regarding the method for designing integrated circuits (ICs) further comprising step of calculating at least one of electrical parameters of IC models, and creating matrix representation for at least one of

electrical parameters, and use it in Dangelo's invention to improve an efficiency of the IC design.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rostoker et al. (US Patent 5,557;531) and US Patent 5,867,399) discloses a methodology that includes using estimators, based on data gathered over a number of realized designs, for partitioning and evaluating a design (based on timing calculating/critical interconnect lines) prior to logic synthesis. From the structural description that is transformed in series to floor plan and schematic (gate level) design, a physical implementation of the device is readily realized.

Beakes et al. (US Patent 6,131,182) teaches a method on a computer system that allows various tile information about the parameterized symbolic and physical views to be determined, including node capacitances, layout dimensions and device parameters. Such properties of the tiles may be generated by software without instantiating tiles and analyzing the mask data or schematics directly by modifying the interconnections between the various macros determined from the floor plan;

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B Levin whose telephone number is 703-305-0144. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 703-308-1323. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

N L

VUTHE SIEK
PRIMARY EXAMINER